REMARKS

This Amendment is filed in response to the FINAL Office Action mailed on November 23, 2005, and in response to the Advisory Action mailed on 28 February 2006, and in the Request for Continued Examination (RCE) filed on even date herewith.

Claims 67-127 are in the case.

Claims 67, 92, 111 and 117 were amended to better claim the invention.

New claims 118 – 127 were added to better claim the invention.

Please enter and consider the Amendment under 37 C.F.R. 1.116 filed on March 4, 2006.

At Paragraphs 5, 7, 8, and 9B of the FINAL Office Action mailed November 25, 2005, Claims 67-72, 78-97, and 104-117 were rejected under 35 U.S.C. 102(b) as being anticipated by Hao, et al. U. S. Patent No. 4,594,665 issued June 10, 1986 (hereinafter Hao).

The present invention, as set forth in representative claim 67, comprises in part:

67. A processor, comprising:

a first execution unit having a first and second input register coupled to first and second inputs to a first arithmetic logic unit (ALU), the first and second input registers of the first execution unit to store source operands, ***the first ALU capable of addressing a memory to retrieve a source operand;***

a second execution unit having a first and second input register, the second register coupled to a second input to a second ALU, the first and second input registers of the second execution unit to store source operands, ***the second ALU not capable of addressing the memory;*** and

a multiplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU, ***the MUX permitting both the first and second ALU to share the source operand retrieved by the first ALU from the memory.***

Hao discloses an apparatus for handling k-instructions at a time in a pipelined processor for parallel execution of inherently sequential instructions. The apparatus uses a first data flow and a second data flow. The first data flow uses a two-input adder, general register, and two staging registers. The second data flow uses a three-input adder (22), a general purpose register, and two input staging registers (25-26).

Hao discloses two ALUs, ALU1 "1" and ALU2 "21". Both of Hao's ALUs connect to general purpose registers GPRs ("4" and "24"), and the GPRs appear to both connect to the same data flow lines. Both of Hao's ALUs appear to be capable of addressing any data as operands from the inputs to his GPRs.

Applicant respectfully urges that Hao does not disclose Applicant's claimed novel:

"A processor, comprising . . . ***a first arithmetic logic unit (ALU) . . . the first ALU capable of addressing a memory to retrieve a source operand . . . a second ALU . . . the second ALU not capable of addressing the memory . . . a multiplexer (MUX) . . . the MUX permitting both the first and second ALU to share the source operand retrieved by the first ALU from the memory.***"

That is, Applicant respectfully urges that Hao has no disclosure of a first ALU which can address a memory to retrieve an operand, and a second ALU which cannot address the memory to retrieve an operand.

Applicant therefore respectfully urges that Hao is legally incapable of anticipating Applicant's claimed novel invention under 35 U.S.C. 102 because of the absence from Hao of Applicant's claimed novel: "A processor, comprising . . . ***a first arithmetic logic unit (ALU) . . . the first ALU capable of addressing a memory to retrieve a source operand . . . a second ALU . . . the second ALU not capable of addressing the memory . . . a multiplexer (MUX) . . . the MUX permitting both the first and second ALU to share the source operand retrieved by the first ALU from the memory.***"

Applicant has added new claims 118 – 127 to better claim the invention.

New claim 118 states:

118. A processor, comprising:
a first ALU, the first ALU capable of addressing a memory to retrieve a source operand from the memory;
a second ALU, the second ALU not capable of addressing the memory; and
a circuit to couple a first input of the first ALU to a first input of the second ALU to provide an operand retrieved from the memory by the first ALU as an input to the second ALU.

Applicant respectfully urges that new claim 118 is allowable because of the absence from all cited art of Applicant's claimed novel ***a second ALU, the second ALU not capable of addressing the memory; and***

a circuit to couple a first input of the first ALU to a first input of the second ALU to provide an operand retrieved from the memory by the first ALU as an input to the second ALU.

Further, new claim 120 states:

120. A processor, comprising:
a first ALU, the first ALU capable of addressing a memory to retrieve an operand
a second ALU, the second ALU not capable of addressing the memory;
a first circuit capable of providing an operand retrieved by the first ALU from a memory as an input to the second ALU;
a second circuit capable of providing a result from either the first ALU or the second ALU as an input to the second ALU; and
an instruction set having a register decode value which is capable of selecting as an input to the second ALU either the operand or the result.

Again, Applicant respectfully urges that claim 120 is allowable because of the absence from all of the cited art of Applicant's claimed novel:

a first ALU, the first ALU capable of addressing a memory to retrieve an operand

a second ALU, the second ALU not capable of addressing the memory.

All independent claims are believed to be in condition for allowance.

All dependent claims are dependent from independent claims which are believed to be in condition for allowance.

Accordingly, all dependent claims are believed to be in condition for allowance.

Favorable action is respectfully solicited.

PATENTS
112025-0167
CPOL# 45681 Seq.# 1503

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

A. Sidney Johnston
Reg. No. 29,548
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500